By: Sajit Chandra Shakya

Preface

How many types of logic Gates do you know?

100, 1000, or 10000.

The more the gates you know, the more you are considered proficient in electronics.

BUT

Do you know the basics of the most elementary gates? It is important since until you know their operation, you would not know the intricate mechanisms of complex circuits of higher order (which would make logic gates appear trivial).

This simple booklet is to enlighten you on the simplest gates.

Expect a lot more from me.

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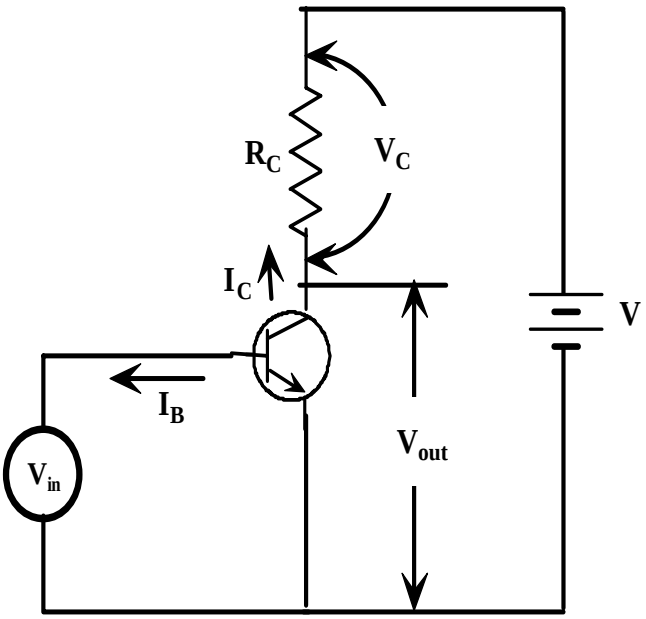
The "NOT" gate



The "NOT" gate is the circuit which gives a high voltage if it is input with low voltage and low voltage if a high voltage is provided. It is constructed with the help of a simple transistor in connection with a voltage source. The input is given to the base-emitter circuit and the output is taken across the collector-emitter. The circuit arrangement for constructing the "NOT" gate would be as in the figure and the truth table as well as overall action can be understood from the accompanying table.

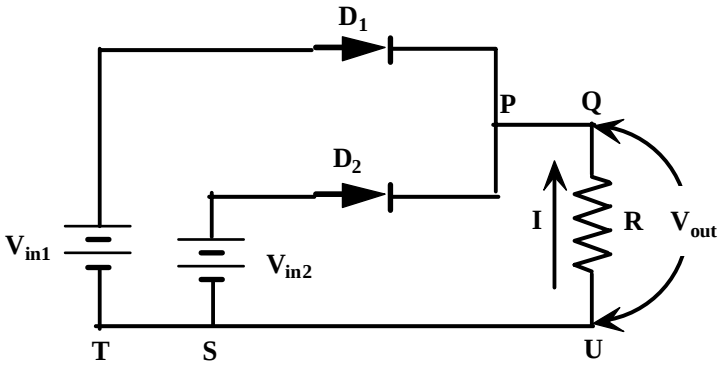
V_{in}	V_{out}
High	**Low**
Low	**High**

Or

V_{in}	V_{out}
1	**0**
0	**1**

When V_{in} is high,	When V_{in} is low,
I_B will be **high**,	I_B will be **low**,
I_C will be **high** ($\because I_C = \beta I_B$),	I_C will be **low** ($\because I_C = \beta I_B$),
V_C will be **high** ($\because V_C = I_C R_C$),	V_C will be **low** ($\because V_C = I_C R_C$),
V_{out} will be **low** ($\because V_{out} = V - V_C$).	V_{out} will be **high** ($\because V_{out} = V - V_C$).

The "OR" gate



The "OR" gate is the circuit consisting of two inputs and an output, in which a high output is obtained if any one of the input is high. The circuit otherwise would give a low output. It is constructed by using two diodes, through which inputs are given and a resistor, across which output is measured. The circuit arrangement for constructing the "OR" gate would be as in the figure and the truth table as well as overall action can be understood from the accompanying tables.

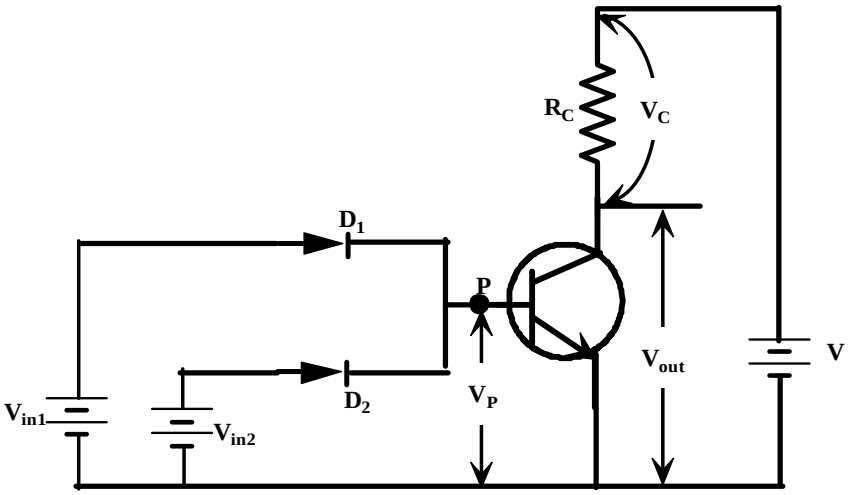
V_{in1}	V_{in2}	V_{out}
Low	Low	**Low**
High	Low	**High**
Low	High	**High**
High	High	**High**

or

V_{in1}	V_{in2}	V_{out}
0	0	**0**
1	0	**1**
0	1	**1**
1	1	**1**

When both V_{in1} and V_{in2} are low,	Both of them are not giving any current, so I is low and V_{out} is **low** ($\because V_{out} = IR$).
When V_{in1} is high and V_{in2} is low,	Diode D_1 will conduct because it is forward biased by V_{in1}. Diode D_2 will not because it is not given any potential difference ($\because V_{in2}$ is low). So electrons from V_{in1} will pass through T, S (they can not go from S to diode D_2 because D_2 is already non-conducting), U, resistor R, Q and reach point P. They can not go through D_2 because it is non-conducting. So they will pass through D_1 to complete a circuit, making the value of current I high, so V_{out} (=IR) will also be **high**.
When V_{in1} is low and V_{in2} is high,	Diode D_2 will conduct because it is forward biased by V_{in2}. Diode D_1 will not because it is not given any potential difference ($\because V_{in1}$ is low). So electrons from V_{in2} will come to S first, where they have two paths; to go towards T or U. They don't go to T because Diode D_1 is not conducting. So they go to U, resistor R, Q and reach point P. So they will pass through D_2 to complete a circuit, making the value of current I high, so V_{out} (=IR) will also be **high**.
When both V_{in1} and V_{in2} are high,	In this case, both the diodes D_1 and D_2 will conduct because both of them are forward biased by V_{in1} and V_{in2}. So electrons from both input sources will combine at S, then go through U, resistor R, Q and to P. Then they distribute themselves along the two paths towards the diodes and then to the cells, completing both the circuits, making the value of current I high, so V_{out} (=IR) will also be **high**.

The "NOR" gate



The "NOR" gate is the circuit consisting of two inputs and an output, in which a low output is obtained if any one of the input is high. The circuit otherwise would give a high output. This type of gate can is constructed by reversing the output of an "OR" gate, so it employs two diodes (for "OR" gate), through which inputs are given, and a transistor to 'reverse' the output given by the combination of the diodes. It also requires a power source to drive the transistor. The circuit arrangement for constructing the "OR" gate would be as in the figure and the truth table as well as overall action can be understood from the accompanying tables.

V_{in1}	V_{in2}	V_p	V_{out}
Low	Low	Low	**High**
High	Low	High	**Low**
Low	High	High	**Low**
High	High	High	**Low**

or

V_{in1}	V_{in2}	V_p	V_{out}
0	0	0	**1**
1	0	1	**0**
0	1	1	**0**
1	1	1	**0**

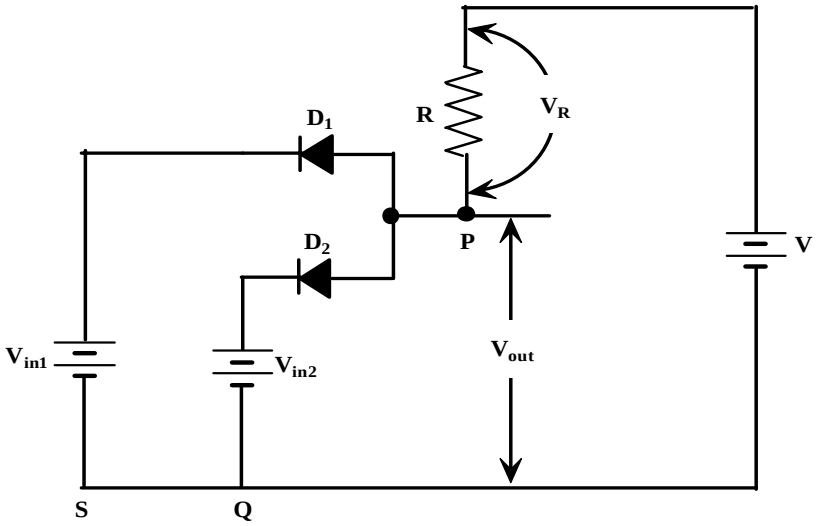
When both V_{in1} and V_{in2} are low,	The value of V_p in this case is low (according to the principles of the "OR" gate), so V_{out} will be **high**.

When V_{in1} is high and V_{in2} is low,	In this case, V_p will be high (according to the principles of the "OR" gate), which will be reversed by the transistor and so V_{out} will be **low**.

When V_{in1} is low and V_{in2} is high,	In this case also, V_p will be high (according to the principles of the "OR" gate), which will be reversed by the transistor and so V_{out} will be **low**.

When both V_{in1} and V_{in2} are high,	In this case also, V_p will be high (according to the principles of the "OR" gate), which will be reversed by the transistor and so V_{out} will be **low**.

The "AND" gate



The "AND" gate is the circuit consisting of two inputs and an output, in which a high output is obtained if both the inputs are high. The circuit otherwise would give a low output. It is constructed by using two diodes, through which inputs are given and a resistor, along with another cell, which is often the driver. The circuit arrangement for constructing the "AND" gate would be as in the figure (to the left) and the truth table as well as overall action can be understood from the accompanying tables.

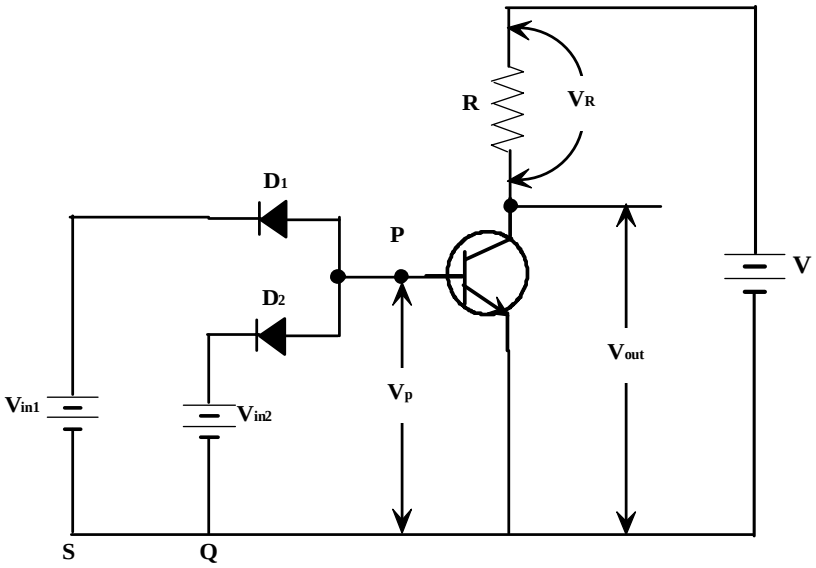
V_{in1}	V_{in2}	V_{out}
Low	Low	**Low**
High	Low	**Low**
Low	High	**Low**
High	High	**High**

or

V_{in1}	V_{in2}	V_{out}
0	0	**0**
1	0	**0**
0	1	**0**
1	1	**1**

When both V_{in1} and V_{in2} are low,	When the potential difference across any device is zero they act as simple wire connections. This is the case with both the input voltage sources V_{in1} and V_{in2}. So the cell V will forward bias both the diodes (because their p sides are connected to the positive terminal of the cell and n sides to the negative). Therefore electrons from the cell V will reach Q and S, travel respectively through D_2 and D_1 to reach P, then through resistor R and again to V. Since the connection across P and Q (also P and S) appear as simple wire connections, there is no potential drop across them. So V_{out} will be **low**.
When V_{in1} is high and V_{in2} is low,	In this case, Diode D_1 will be reverse biased by V_{in1}, So it becomes non-conducting. However V_{in2} still acts as a simple connection (because it is still zero). So when electrons from V reach Q they can not go through D_1. So they go through D_2. The path between P and Q still appear as simple wire connection. Therefore there is no potential drop across P and Q. So V_{out} will be **low** again.
When V_{in1} is low and V_{in2} is high,	In this case, Diode D_2 will be reverse biased by V_{in2}, So it becomes non-conducting. However V_{in1} acts as a simple connection (because it is zero). So when electrons from V reach Q they can not go through D_2. So they go to S and through D_2. The path between P and S appear as simple wire connection. Therefore there is no potential drop across P and S, which is the same as across P and Q. So V_{out} will be **low** again.
When both V_{in1} and V_{in2} are high,	In this case, both the diodes D_1 and D_2 will be reverse biased by V_{in1} and V_{in2}. So both of them can not conduct. So electrons get stuck after reaching Q and subsequently S, as if there is a break across P and Q (also across P and S). So the resistance R_{PQ}, which is the resistance across P and Q; and also equal to R_{PS} (the resistance across P and S); will be infinite. So whatever high the value of R is, R_{PQ} and R_{PS} will be very high compared to R. So V_{out} will be **high**.

The "NAND" gate



The "NAND" gate is the circuit consisting of two inputs and an output, in which a low output is obtained if both the inputs are high. The circuit otherwise would give a high output. It is constructed by using two diodes, through which inputs are given and which collectively form the "AND" gate. The output of the "AND" gate is then reversed by using a "NOT" gate made of a transistor in conjunction with a resistor and a driver cell. The circuit arrangement for constructing the "NAND" gate would be as in the figure (to the left) and the truth table as well as overall action can be understood from the accompanying tables.

V_{in1}	V_{in2}	V_p	V_{out}
Low	Low	Low	**High**
High	Low	Low	**High**
Low	High	Low	**High**
High	High	High	**Low**

or

V_{in1}	V_{in2}	V_p	V_{out}
0	0	0	**1**
1	0	0	**1**
0	1	0	**1**
1	1	1	**0**

When both V_{in1} and V_{in2} are low,	When both V_{in1} and V_{in2} are low, V_p will be low (according to the behavior of "AND" gate). So V_{out} will be **high** (according to the behavior of "NOT" gate).
When V_{in1} is high and V_{in2} is low,	When V_{in1} is high but V_{in2} is low, V_p will be low. So V_{out} will be **high**.
When V_{in1} is low and V_{in2} is high,	When V_{in2} is high but V_{in1} is low, V_p will be low. So V_{out} will be **high**.
When both V_{in1} and V_{in2} are high,	When both V_{in1} and V_{in2} are high, V_p will be high (according to the behavior of "AND" gate). So V_{out} will be **low** (according to the behavior of "NOT" gate).

These were the simplest gates. All the other gates can be made of these gates by several possible combinations which are numerous in number.

I hope that you will take a firm footing and explore higher grounds.

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